Claims

[c1] What is claimed is:

1.A method of forming a system on chip (SOC), the method utilizing nitride read only memory (NROM) to establish read only memory (ROM) and non-volatile memory, a substrate of the system on chip comprising a memory area and a periphery area, the memory area further comprising a non-volatile memory area and a read only memory area, the read only memory area further comprising at least a low threshold voltage (low V_{th}) device area and a high threshold voltage (high V_{th}) device area, the method comprising:

forming a plurality of field oxide layers on the surface of the substrate so as to form an isolator of each device in the periphery area, the non-volatile memory area, and the read only memory area, respectively, and to define the active area of each device;

forming an ONO dielectric layer on the surface of the substrate, the ONO dielectric layer comprising a bottom oxide layer, a silicon nitride layer, and a top oxide layer;

forming a first photoresist layer on the surface of the ONO dielectric layer, and performing a first lithography process so as to define sites for a plurality of bit lines;

performing a first etching process, the first etching process utilizing the first photoresist layer as a mask so as to remove the top oxide layer and the silicon nitride layer and part of the bottom oxide layer not covered by the first photoresist layer;

performing a first ion implantation process so as to form a plurality of N-type doping areas, and each of the buried bit lines in the memory area;

removing the first photoresist layer;

performing a thermal oxidation process so as to form a buried drain oxide layer atop the surface of each buried bit line;

forming first a polysilicon layer and then a second photoresist layer on the surface of the substrate so as to define sites of a plurality of word lines in the memory area and a plurality of gates in the periphery area in the second photoresist layer by utilizing a second lithography process;

performing a second etching process to simultaneously remove the polysilicon

layer not covered by the second photoresist layer and form each of the word lines in the memory area and each gate of the periphery transistor in the periphery area, so as to form at least one NROM in the non-volatile memory area, a low threshold voltage(low V_{th}) device in the low threshold voltage device area of the read only memory area, and a high threshold voltage(high V_{th}) device in the high threshold voltage device area in the read only memory area; and

removing the second photoresist layer.

[c2] 2. The method of claim 1 wherein the substrate is a silicon substrate.

[c3] 3. The method of claim 1 wherein the bottom oxide layer is formed by utilizing a low temperature oxidation process with a temperature ranging from 750 ° C to 1000 ° C and a thickness ranging from 20 Å (angstroms) to 150 Å .

[c4] 4. The method of claim 1 wherein the silicon nitride layer is formed by utilizing a low pressure vapor deposition(LPCVD) process, for use as a floating gate of the NROM, and has a thickness ranging from 50 Å (angstroms) to 300 Å .

[c5] 5. The method of claim 1 wherein the top oxide layer is formed by utilizing a wet oxidation process with a thickness ranging from 50 Å (angstroms) to 200 Å .

[c6] 6. The method of claim 1 wherein the method further comprises an ion implantation process for adjusting a threshold voltage of each periphery transistor.

[c7] 7. The method of claim 6 wherein the ion implantation process is performed before forming the ONO dielectric layer.

[c8] 8. The method of claim 6 wherein the ion implantation process is performed after forming the ONO dielectric layer.

[c9] 9. The method of claim 1 wherein the method further comprises a first angled ion implantation process and a second angled ion implantation process so as to form a P-type pocket doping area at two relative sides of each bit line.

[c10] 10. The method of claim 9 wherein the first angled ion implantation process and a second angled ion implantation process are performed before the first ion implantation process.

[c11] 11. The method of claim 9 wherein the first angled ion implantation process and a second angled ion implantation process are performed after the first ion implantation process.

[c12] 12. The method of claim 1 wherein the method further comprises a third etching process so as to remove the ONO dielectric layer on the active area in the periphery area.

[c13] 13. The method of claim 12 wherein the thermal oxidation process simultaneously forms at least a silicon oxide layer on the surface of the active area in the periphery area for use as the gate oxide layer of each periphery transistor.

[c14] 14. The method of claim 13 wherein after removing the ONO dielectric layer and before forming the gate oxide layer the method further comprises:
performing a third lithography process so as to form a patterned third photoresist layer, the third photoresist layer covering the low threshold voltage (low V_{th})device in the read only memory area, the nitride read only memory area and the periphery area;
performing an ion implantation process for threshold voltage adjustment, implanting P-type dopant into the high threshold voltage device to adjust the threshold voltage of the high threshold voltage device and complete a ROM code process; and
removing the third photoresist layer.

[c15] 15. The method of claim 14 wherein the third photoresist layer covers each bit line.

[c16] 16. The method of claim 1 wherein after removing the second photoresist layer the method further comprising:
performing a fourth lithography process so as to form a patterned fourth photoresist layer, the fourth photoresist layer covering the low threshold

voltage(low V_{th})device in the read only memory area, the nitride read only memory area and the periphery area;

performing an ion implantation process for threshold voltage adjustment, implanting P type dopant into the high threshold voltage device to adjust the threshold voltage of the high threshold voltage device and complete the ROM code process; and

removing the fourth photoresist layer.

[c17] 17. The method of claim 1 wherein after forming the polysilicon layer and before etching the polysilicon layer the method further comprising:

performing a fifth lithography process so as to form a patterned fifth photoresist layer, the fifth photoresist layer covering the low threshold voltage (low V_{th})device in the read only memory area, the nitride read only memory area and the periphery area;

performing an ion implantation process for threshold voltage adjustment, implanting P type dopant into the high threshold voltage device to adjust the threshold voltage of the high threshold voltage device and complete the ROM code process; and

removing the fifth photoresist layer.

[c18] 18. The method of claim 1 wherein a polysilicide layer is formed on the surface of the polysilicon layer.

[c19] 19. The method of claim 1 wherein the high threshold voltage device and the low threshold voltage device are for presenting 0&1 or 1&0 respectively so as to store a specific information or data.

[c20] 20. The method of claim 1 wherein the read only memory area is a mask read only memory(mask ROM, MROM) area.